REMARKS

Claims 1-27 are pending in the present application. Claims 1-3, 5-7, 10-12, 14-16, 19-21, and 23-25 were amended. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102, Anticipation, Claims 1-27

The examiner has rejected claims 1-27 under 35 U.S.C. § 102(a) and 35 U.S.C. § 102(e) as being anticipated by *Wall et al.* (U.S. Patent No. 6,507,923). This rejection is respectfully traversed.

As per the Office Action, the examiner states:

> With respect to claims 1, 10 and 19, Wall et al. teach an integrated multi-channel Fibre channel analyzer provides coordinated and cooperative triggering and capturing of data cross multiple channel in the fibre channel network for testing the error handling capabilities of the system's firmware (abstract and column 6, lines 6-16) comprising defining a specific system event to be monitored (column 5, lines 34-40 and column 6, lines 16); creating a trigger in analyzer, wherein the trigger is used to allow the analyzer to capture information related to the specific system event (column 5, line 60 to column 6, line 6); recciving a signal at the analyzer, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed (abstract and column 2, line 31 to column 3, line 20 and column 5, line 60 to column 6, line 6).

(Office Action dated April 22, 2005, pages 2 and 3-4).

A prior art reference anticipates the claimed invention under 35 U.S.C. §102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). The *Wall* reference cited by the examiner does not anticipate the present invention as recited in claims 1, 10, and 19, because *Wall* fails to teach each and every element of the claims. Independent claim 1, which is representative of independent claims 10 and 19 with regard to similarly recited subject matter, recites:

> 1. A method for testing the error handling capabilities of a system's firmware by allowing an analyzer to trigger on a specific system event, comprising:

defining a specific system event to be monitored;
creating a trigger configured to allow an analyzer to capture information related to the specific system event, wherein the trigger is controlled by an intelligent triggering controller external to the analyzer; and
receiving a signal at the analyzer from the intelligent triggering controller, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed.

Wall does not teach the features emphasized above. As discussed in the Abstract, *Wall* teaches an integrated multi-channel analyzer that provides coordinated and cooperative triggering and capture of data across multiple fibre channels. Two or more devices are monitored on a fibre channel loop in an integrated manner to allow for combinatorial triggering across multiple ports. The *Wall* system allows for controlling triggering decisions across multiple analyzer channels by having the status conditions of each analyzer channel propagated to all other analyzer channels. Trace data is captured in trace buffer memories, analyzed, and the resident processor sends the relevant trace data to a remote host processor upon receiving a command from the remote host processor.

The Examiner alleges that *Wall* teaches creating a trigger configured to allow an analyzer to capture information related to the specific system event, wherein the trigger is controlled by an intelligent triggering controller external to the analyzer in the following cited sections of *Wall*:

> The bus 40 enables the host processor to set up triggering and filtering conditions within each channel logic 32, 34 and to download captured trace data from the buffers 36, 38. There is a pair of internal cross-channel connections 26, 28 between the channels 22, 24 that can selectively transfer data between the channels 22, 24. In addition to the bus 40, internal traces or interconnections 44 between channel logic 32, 34 are typically provided for on the circuit board 30 to coordinate the operation of the two channels 22, 24. In the paired channel approach utilized by the prior art, both of the channels 22, 24 must meet the predetermined trigger condition for that channel in order for the analyzer 20 to be triggered to capture the recorded data packets in both of the trace memories 36, 38.

(*Wall*, col. 5, line 60 to col. 6, line 6).

> Analysis of the data captured by the integrated multi-channel analyzer is enhanced by a processor resident in the cabinet that is connected by a data/control bus to each analyzer channel and its associated trace buffer memory. The resident processor receives high level commands from a remote host processor and coordinates the way in which the analyzer channels are configured to monitor the Fibre Channel network. Once trace data is captured in one or more of the trace buffer memories, the resident processor coordinates the transfer of relevant portions of the trace data to the remote host processor. To reduce the amount of data that must be transferred to the remote host processor, each analyzer channel preferably includes a hardware search engine that can quickly and efficiently identify relevant data patterns in the trace buffer memory. Once the trace data has been captured in the trace buffer memories, the resident processor initiates a time indexing routine that uses the hardware search engine in each analyzer channel to index the trace data for that analyzer channel.

(*Wall*, col. 3, lines 10-28).

The first passage above teaches that predetermined triggering and filtering conditions are set up within each channel logic located in the analyzer. When a channel meets a triggering condition, the analyzer is triggered to capture the recorded data packets in the trace buffers of the analyzer. However, there is no mention in this cited section that the trigger is controlled by an intelligent triggering controller external to an analyzer. To the contrary, the passage merely describes the shortcomings of a paired channel approach in the prior art, wherein the paired channel approach requires that both channels must meet the predetermined trigger conditions for each channel in order for the analyzer to be triggered to capture the data of interest.

The second passage above teaches that a processor residing in the analyzer is connected by a data/control bus to each analyzer channel. The resident processor receives high level commands from a remote host processor and coordinates the way in which the analyzer channels are configured to monitor the Fibre Channel network. However, these commands from the remote host processor merely instruct the resident processor to send relevant portions of the trace buffer memory to the remote host processor (*Wall*, col. 9, lines 37-45; col. 9, line 62 to col. 10, line 2), wherein the relevant portions are determined using the parameters provided by the host processor (*Wall*, col. 9, lines 37-45). There is no mention in *Wall* that the host processor triggers the analyzer to capture data; rather,

the analyzer generates the triggers and the host processor merely requests the data that has already been captured by the analyzers. Rather, when an analyzer channel in *Wall* detects a particular condition, the analyzer channel triggers the capture of trace data of interest, and synchronizes the triggering of mechanisms internal to the analyzers.

In contrast, claim 1 of the present invention recites that the trigger is controlled by an intelligent triggering controller external to the analyzer. For example, as disclosed at least on page 11, lines 17-19 of the present specification, this external intelligent triggering controller may be a host system, a storage device, or a peer communications device. Having the external triggering controller generate a trigger for the analyzer provides the ability to stop the analyzer from gathering additional system activity information, since internal states of the firmware are not necessarily observable to the analyzer in a reasonable amount of time to preserve the useful information for debug purposes or may be misinterpreted by the OS driver layers. Generating a trigger external to the analyzers allows for monitoring firmware states based upon OS, host bus adapter, or other data. Thus, the present invention as recited in claim 1 provides the capability in embedded firmware or at the OS level to generate a trigger to tell the analyzers when to capture data. This trigger is incapable of being generated by the analyzers, since there are internal firmware states that are unobservable to the analyzers. Thus, *Wall* does not teach creating a trigger configured to allow an analyzer to capture information related to the specific system event, wherein the trigger is controlled by an intelligent triggering mechanism external to the analyzer, as recited in claims 1, 10, and 19 of the present invention.

The Examiner also alleges that *Wall* teaches receiving a signal at the analyzer from the intelligent triggering controller, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed in column 5, line 60 to column 6, line 6 (reproduced above), and column 2, line 31 to column 3, line 20, which is reproduced below:

> Once this type of multiple analyzer arrangement in the prior art has been set up and triggered, data from the two analyzers is time correlated by a time stamping arrangement to allow for comparison by a host

processor of data captured by the pair of channels in the first analyzer with the data captured by the pair of channels in the second analyzer. The time stamped data is then separately downloaded from each analyzer and the host processor is used to correlate arid evaluate the captured data. Examples of the use of time stamping to coordinate multiple communication analyzers for communication interfaces other than a Fibre Channel protocol are shown in U.S. Pat. Nos. 5,535,193 and 5,590,116. U.S. Pat. Nos. 5,276,579 and 5,375,159 describe examples of protocol analyzers for telecommunication data networks that include the ability to remotely operate and coordinate the analyzers. U.S. Pat. No. 5,600,632 describes performance monitoring using synchronized network analyzers in which the data from all of the analyzers is aggregated and sorted chronologically before it is analyzed.

While existing Fibre Channel analyzers are adequate for trouble shooting single Fibre Channel devices, there is a need for a Fibre Channel analyzer that addresses the problems of existing Fibre Channel analyzers when attempting to analyze complicated, large multi-device Fibre Channel networks and provides for a more integrated solution to analyzing large and complicated Fibre Channel networks.

SUMMARY OF THE INVENTION

The present invention is an integrated multi-channel Fibre Channel analyzer that provides coordinated and cooperative triggering and capture of data across multiple channels in a Fibre Channel network. The integrated multi-channel analyzer accommodates up to sixteen separate analyzer channels in a single cabinet. Each analyzer channel is comprised of an input port connection to the Fibre Channel network, a trace buffer memory that captures data and logic circuitry that controls the operation of the trace buffer memory in response to a status condition. A high speed status bus is connected to each analyzer channel and propagates the status conditions of each analyzer channel to all other analyzer channels. In this way, the integrated multi-channel analyzer allows for distributive control over triggering decisions across multiple analyzer channels, and also allows for multi-level triggering where different conditions may be detected by different analyzer channels.

Analysis of the data captured by the integrated multi-channel analyzer is enhanced by a processor resident in the cabinet that is connected by a data/control bus to each analyzer channel and its associated trace buffer memory. The resident processor receives high level commands from a remote host processor and coordinates the way in which the analyzer channels are configured to monitor the Fibre Channel network. Once trace data is captured in one or more of the trace buffer memories, the resident processor coordinates the transfer of relevant portions of the trace data to the remote host processor.

(*Wall*, col. 2, line 31 to col. 3, line 20).

As previously mentioned, the first cited passage (column 5, line 60 to column 6, line 6) teaches predetermined triggering and filtering conditions are set up within each channel logic located in the analyzer.

The second cited passage (col. 2, line 31 to col. 3, line 20) describes when the multiple analyzer arrangement is triggered, trace data captured by the two analyzers is time correlated by a time stamping arrangement. This time correlation allows the host processor to compare the data captured by the pair of channels in a first analyzer with the data captured by the pair of channels in a second analyzer. The time stamped data is separately downloaded from each analyzer and the host processor is used to correlate and evaluate the captured data. However, *Wall* does not teach that the analyzer receives a signal from the intelligent triggering controller, and that this signal triggers the analyzer to capture data related to the specific system event. As mentioned above, the intelligent triggering controller is external to the analyzer. Thus, rather than having an analyzer provide self-generated logic signals to trigger data capture, claim 1 of the present invention recites that the signal to trigger the analyzer to capture trace data is provided by the external intelligent triggering controller. Consequently, using data from external sources to generate the trigger on the analyzer allows for capturing trace data for a specific system event and within a time period adequate for the analyzer to capture useful data for the specific system event. Thus, *Wall* does not teach receiving a signal at the analyzer from the intelligent triggering controller, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed, as recited in claims 1, 10, and 19 of the present invention.

Furthermore, *Wall* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. *Wall* actually teaches away from the presently claimed invention because it teaches a multi-channel analyzer that coordinates cooperative triggering and data capture across multiple fibre channels as opposed to an intelligent triggering controller external to the analyzer that controls the signal to trigger data capture as in the presently claimed invention. Absent the examiner pointing out some teaching or incentive to implement *Wall* and the intelligent triggering

controller external to the analyzer of the present invention, one of ordinary skill in the art would not be led to modify *Wall* to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify *Wall* in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

In view of the above, Applicants respectfully submit that *Wall* fails to teach the features of claims 1, 10, and 19. At least by virtue of their dependency on claims 1, 10, and 19, respectively, *Wall* also does not teach the features of dependent claims 3-9, 12-18, and 21-27. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 1-27 under 35 U.S.C. §102.

Furthermore, these dependent claims include additional features not found in *Wall*. For example, claims 2, 11, and 20 of the present invention recite wherein the intelligent triggering controller is one of a host system, a storage device, or a peer communications device, and claims 3, 12, and 21 of the present invention recite wherein the intelligent triggering controller is a fibre channel host bus adapter in the host system. *Wall* makes no mention of a host system (or host bus adapter), storage device, or peer communications device controlling the trigger. In another example, claims 5, 14, and 23 recite that the fibre channel host bus adapter maps all connected devices logically to determine status conditions of all the connected devices. Again, as *Wall* does not mention a host bus adapter controls the trigger in the analyzer, it follows that *Wall* also does not teach that the host bust adapter maps devices logically and knows the status conditions of the devices. This host bust adapter data may be used to control the analyzer to trigger on a specific event. Moreover, claims 6, 15, and 24 recite wherein the intelligent triggering controller controls the trigger in the analyzer to capture and store data regarding internal states of the system's firmware. The multi-channel analyzer in *Wall* does not teach this feature, as the analyzer in *Wall* is incapable of generating such a special trigger, as there are firmware states that the analyzer cannot observe. In contrast, by having the intelligent trigger controller generate a trigger external to the analyzer to instruct the analyzer to capture data for the specific event, these firmware states may be tracked using the present invention. Claims 8, 17, and 26 recite wherein the fibre channel

host bus adapter includes a number of output pins, and wherein each output pin may be programmed with a separate triggering mechanism. As *Wall* does not teach a host bus adapter as the intelligent triggering mechanism in claim 3 from which claim 8 depends, *Wall* cannot teach a host bus adapter with a number of output pins programmed with a separate triggering mechanism.

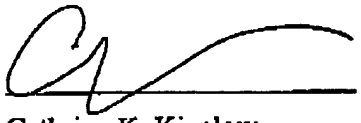
II. Conclusion

It is respectfully urged that the subject application is patentable over *Wall* and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 7/20/05

Respectfully submitted,



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